ABSTRACT OF THE DISCLOSURE

Circuitry is provided for controlling the slew rate of a negative output supply. The slew rate control circuitry includes an NMOS FET, a feedback resistor connected across the drain and the gate of the NMOS FET, an input resistor connected to the gate of the NMOS FET, level shifting circuitry connected between a positive output supply voltage and the input resistor, and a bias current source connected to the gate of the NMOS FET. A negative input supply voltage is connected to the source of the NMOS FET, and the negative output supply voltage is provided across a load connected to the drain of the NMOS FET. As the positive supply voltage ramps up from 0 to $+V_S$, the level shifter provides a voltage to the input resistor that ramps up from $-V_S$ to 0 volts. Further, the drain voltage of the NMOS FET ramps down from 0 to $-V_S$, thereby providing a negative output supply voltage $-V_S$ with a slew rate that linearly tracks the slew rate of the master positive output supply.

299379

ATTORNEY DOCKET NO. TI-36859 (UNITI-173XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313